DESIGN NOTES

Single IC, Five Output Switching Power Supply System for Portable Electronics – Design Note 150

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The drive for higher performance portable electronic systems, concomitant with the need to remain compatible with existing interfacing standards and hardware, has caused the number of system power supply voltages to proliferate. This Design Note describes how to generate five separate output voltages using the LTC®1538-AUX, a dual synchronous switching regulator controller with internal circuitry adaptable to many additional configurations. The five output voltages chosen in this example are:

- 5V ±4%/25mA linear regulator, which remains active regardless of the state of the switching regulator controllers
- 5V ±2%/3A synchronous switching buck regulator
- 3.3V ±2%/6A synchronous switching buck regulator
- 2.9V ±5%/3A peak low dropout linear regulator deriving power from the 3.3V output
- 12V ±5%/200mA synchronously rectified flyback output deriving power from the 5V output

The 100µA quiescent current, 5V standby linear regulator can efficiently power "wake-up" circuitry in portable systems and can deliver 25mA.

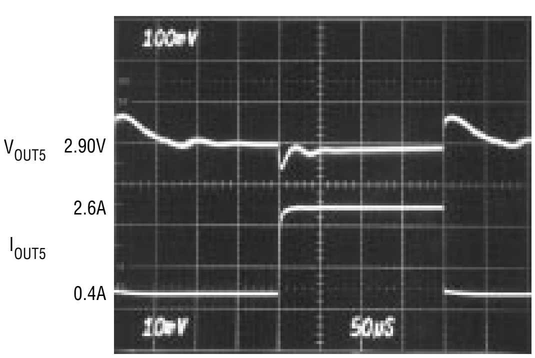

Figure 1. 2.9V Output Transient Load Step Performance

The 5V and 3.3V switching regulators, independently activated by the two RUN/SS pins, provide very efficient, constant frequency operation. This is accomplished by using a synchronous-buck architecture at high currents and switching over to Burst Mode™ operation below approximately 10% to 15% of maximum current, as determined by the current sensing resistor for each controller.

The 5V output from the first controller, or any external voltage between 4.8V and 10V, can be tied to the $ExtV_{CC}$ pin. The power and voltage from this external source will supplant the internal 5V linear regulator if the applied voltage is greater than 4.8V. This technique improves efficiency by eliminating the power dissipated by the IC due to the current drawn through the internal linear regulator and the (V_{IN} – 5V) voltage drop.

The 2.9V linear regulator draws power from the 3.3V output and performs the function of a wide bandwidth, low dropout linear regulator having dynamic performance as illustrated in Figure 1.

The regulator's dominant pole is set by the output capacitance and the load resistance. The loop is stable, provided there is some ESR (0.02Ω to 0.1Ω) in the output capacitor in order to generate phase lead prior to the unity-gain crossover frequency. The AVX-TPS tantalum capacitor used here, or a Sanyo OS-CON type capacitor, has a complex impedance characteristic, providing close to zero phase shift at the unity-gain cross frequency of the amplifier.

The 12V/200mA output uses a synchronously driven, tightly coupled secondary winding on the first controller's primary winding to generate a highly efficient output with a ±5% tolerance under all load and line conditions. The output voltage is fed back to the SFB1 input pin and compared with the internal 1.19V reference. This feedback forces the primary controller into a "forced synchronous" mode, regulating the 12V output regardless of the loading of the primary 5V regulator. Tighter regulation and less ripple can be attained with a slightly higher turns ratio and an additional linear regulator.

Figure 2 shows the overall efficiency for the circuit shown in Figure 3. The $I_{2.9}$ = Proportional curve documents efficiency when all outputs are loaded proportionally to their peak design loads of: 5V at 3A, 3.3V at 3A, 2.9V at 3A and 12V at 200mA. As an example, overall efficiency drops to 90% when the 2.9V output is loaded with 1A (33% of the designed maximum load). For this same efficiency point, the three other outputs are loaded as follows: 5V at 1A, 3.3V at 1A and 12V at 67mA. For the peak load of 36W, as specified above, efficiency drops to 85%.

The $I_{2.9}$ = 0 curve shows efficiency when all outputs are loaded proportional to their peak loads *except* the 2.9V output which is not loaded. This curve documents a 100% design load of 27.3W. The circuit's efficiency peaks for this curve at 95% when the 5V and 3.3V outputs are loaded with 1A and the 12V output is loaded with 67mA.

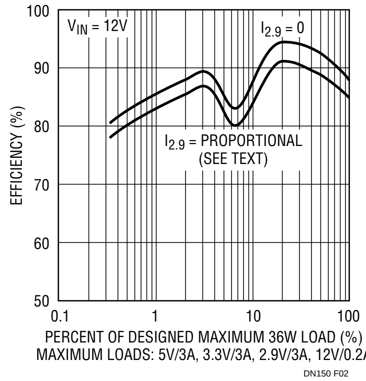

Figure 2. Efficiency vs Percent of the Designed Maximum Load

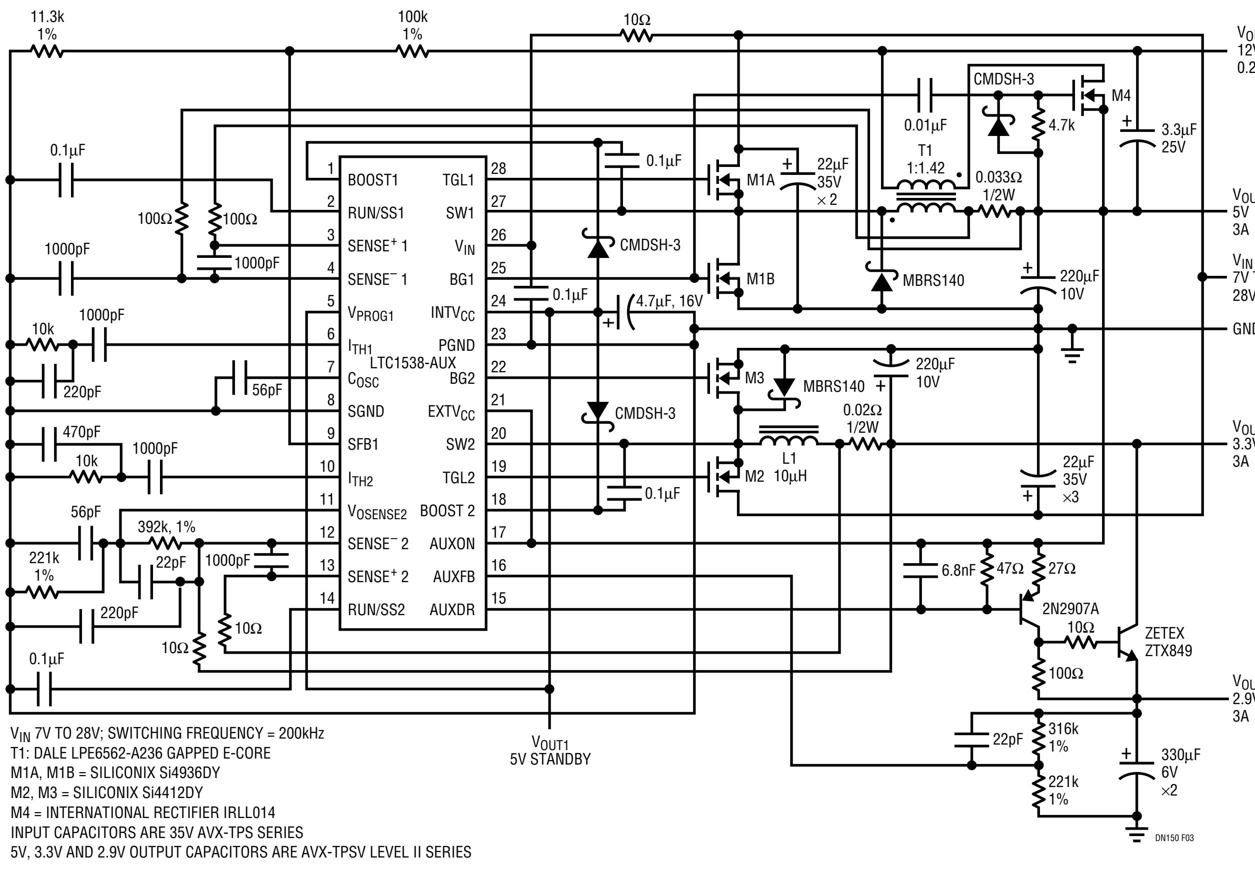

Figure 3. Schematic Diagram of System

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